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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2153	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,045	BOOTH ET AL.	
	Examiner	Art Unit	
	Yasin M. Barqadle	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Applicant's arguments filed on October 01, 2007 have been considered and are not deemed persuasive except for the 101 rejection.

- Claims 1-34 are presented for examination.

Response to Arguments

2. In essence the Applicant argues that :Agilent does not disclose that the test instrument can vary data rate; instead it merely discloses that the test instrument can generate a faction of main clock rate... Agilent does not vary the data rate based on the number of data lane interfaces actively transmitting or actively receiving." page 16, second paragraph.

Examiner respectfully disagrees. For example, Agilent teaches "Figure 7 shows ... . BER testing may be performed at either the XAUI electrical I/O or the 10.3125 Gb/s optical I/0. The internal elastic buffer in the transceiver module or ASIC is effectively disabled by driving the device under test (PUT) with synchronous clocks at 3.125 Gb/s and 10.3125 Gb/s. The presence of the scrambler and de-scrambler makes it very difficult to define a test pattern which could be used

to test BER from the XAUI interface (4 x 3.125 Gb/s) to the 10.3125 Gb/s optical output. Although disabling the scrambler of the OUT via its MDIO management interface would seem to offer a work around, in fact this results in unscrambled idle patterns (see below) with inadequate timing information being supplied to the internal clock and data recovery circuit of the DUT. The testing philosophy described in this document therefore assumes that testing of Xenpak devices is carried out electrically at the 3.125 Gb/s XAUI input and output ports, and separately at the 10.3125 Gb/s optical input and outputs. The XAUI interface is intended for interconnection between ICs; it is a low swing AC coupled differential interface. The AC coupling allows for interoperability between components operating from different supply voltages. The XAUI signal paths are point-to-point connections; each path corresponds to a XAUI lane and comprises two complementary signals making a balanced differential pair. There are four differential paths in each direction - or sixteen connections. These paths are intended to operate up to approximately 50 cm over controlled impedance traces on standard FR4 printed circuit boards. The XAUI inputs of the device under test may be driven single-ended, for example by the Agilent Technologies 71612C pattern generator sub-rate outputs, however some measurements, such as jitter tolerance may benefit by using baluns on

each input when driven from a single-ended source." Page 10. This clearly indicates that Agilent does vary the data rate based on the number of data lane interfaces actively transmitting or actively receiving.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 9-13, and 16-19 are rejected under 35 U.S.C. 102 (b) as being anticipated by Agilent Technologies product notes (Dated January 2002, hereafter referenced as "Agilent").

For claim 1:

A media access controller (MAC) (Figure 1, Data link mapped to MAC and LLC); and

A communication device comprising:

A media independent interface (MII)(Figure 1, XGMII) coupled to the MAC (Figure 1, XGMII is coupled to the MAC by data lines)

a plurality of data lane interfaces (Figure 3 from left, device 1' consists of two blocks from left, let side of XAUI interface and device 2 consists the rest of the blocks right side of XAUI interface, XAUI interfaces are plurality of data lane interfaces) each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane (see the number of XAUI interface line descriptions of XAUI interface is being 16 Point to point, i.e. (4 Tx + 4Rx) times 2 for differential) in a device-to-device interconnection; and

logic to vary the data rate based, a least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection (Variance of data rate is a functional limitation, because no structural element of the logic was claimed in the

claim, therefore reference only need to be capable varying the data rate. The reference is a product note using instruments to test 10GB Ethernet, where the instrument(s) is capable of generating **1/4** main clock rate (see 71612C technical specifications, page 7, sub clock & data Outputs, Specifications: Frequency range **1/4** main clock rate), therefore, the instrument will be able to generate and capture various data rates on the XAUI interface data lines) when viewed in conjunction with the description of, "The XAUI inputs of the device under test may be driven single-ended, for example by the Agilent Technologies 71612C pattern generator *sub-rate* outputs, ...", page 10).

For claim 2:

The system of claim 1 (see supra for discussion), wherein the system further comprises a switch fabric coupled to the MAC (See Figure 7, XAUI on the left hand side coupled to MAC as shown in Figure 2, and switch fabric shown as, i. 16:1 mux along with clock and associated logic (muxes do not have clocks, a control logic built in to convert 8 data input ingress ports to

one egress data output port along with clock) ii. 1:16 demux along with associated control logic (dmuxes does not have clock as input) having an ingress of 1 data and clock with an egress of 8 ports of data output).

For claim 3:

The system of claim 1 (see supra for discussion), wherein the system further comprises a packet classification device coupled to the MAC (see Figure 1, MAC is coupled to higher layers which are capable of classifying the packets, for example in the case of transport layer based on port numbers, etc).

For claim 4:

A device comprising:

a media independent interface (MII) to at least one of transmit and receive data at a data rate (see figure 6, page 9);

a plurality of data lane interfaces (see Figure 6), each data lane interface being capable of at least one of transmitting the serial data signal to and receiving a serial data signal from a data lane

in a device-to-device interconnection (see Figure 6, SCD connector technology); and

logic to vary the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection (Variance of data rate is a functional limitation, because no structural element of the logic was claimed in the claim, therefore reference only need to be capable varying the data rate. The reference is a product note using instruments to test 10GB Ethernet, where the instrument(s) is capable of generating % main clock rate (see 71612C technical specifications, page 7, sub clock & data Outputs, Specifications: Frequency range % main clock rate), therefore, the instrument will be able to generate and capture various data rates on the XAUI interface data lines) when viewed in conjunction with the description of, "The XAUI inputs of the device under test may be driven single-ended, for example by the Agilent Technologies 71612C pattern generator ***sub-rate*** outputs, ...", page 10, last Para).

For claim 5:

the device of claim 4 (see supra for discussion), wherein each data lane interfaces is associated with a first differential pair to transmit a serial data signal and a second differential pair to receive a serial data signal (see Figure 3.10 or Figure 4 of page 8, that shows Differential input and output data lanes).

For claim 6:

The device of claim 5 (see supra for discussion), wherein the plurality of data lane interface are capable of transmitting data to and receiving data from a 10 gigabit attachment unit interface (See Figure 7, XAUI Interface).

For claim 7:

The device of claim 4 (see supra for discussion), wherein the device further comprises:

a plurality of 8B 10B decoders, each 8B 10B decoder being associated with one of the data lane interfaces, each 8B 10B decoder being capable of decoding one eight bit byte from a

differential pair on first intervals of a first clock signal (see Figure 6 or 5, 8B/10B interfaces);

For claim 9:

The device of claim 4, wherein the device-to-device interconnection comprises printed circuit board traces (see page 7, third Para, last line, "XAUI solutions together with the XGP will enable efficient low-cost 10 Gigabit Ethernet direct multiport MAC to optical module interconnects with only ***PC board traces between").***

For claim 10:

The device of claim 4 (see supra for discussion), wherein the device-to-device interconnection comprises a cable (See Figure 3.10 or 4, Opto, Optical interfaces, typically connected by cable).

For claim 11:

A method comprising:

at least one of transmitting data to and receiving data from a media independent interface (MII) at a data rate (see Figure 4);

at least one transmitting a serial data signal to and receiving a serial data signal from one or more data lanes in a device-to-device interconnection, each • data lane being coupled to the MII by an associated data lane interface (see Figure 4, serdes); and

varying the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection (Variance of data rate is a functional limitation, because no structural element of the logic was claimed in the claim, therefore reference only need to be capable varying the data rate. The reference is a product note using instruments to test 10GB Ethernet, where the instrument(s) is capable of generating % main clock rate (see 71612C technical specifications, page 7, sub clock & data Outputs, Specifications: Frequency range **1/4** main clock rate), therefore, the instrument will be able to generate and capture various data rates on the XAUI interface data lines) when viewed in conjunction with the description of, "The XAUI inputs of the device under test may be driven single-ended, for example by the Agilent

Technologies 71612C pattern generator *sub-rate* outputs, ...", page 10, last Para).

For claim 12:

The method of claim 11 (see supra for discussion), the method further comprising:

transmitting one or more serial data signals to the device-to-device interconnection in a first differential pair signal (see Figure 4 or 3); and

receiving one more serial data signals from the device-to-device interconnection in a second differential pair signal(see Figure 4 or 3).

For claim 13:

The method of claim 12 (see supra for discussion), the method further comprising transmitting data to and receiving data from a 10 gigabit attachment unit interface (see Figure 7, XAUI interface).

For claim 16:

The method of claim 11 (see supra for discussion), wherein the device-to-device interconnection comprises printed circuit board traces(see page 7, third Para, last

line, "XAUI solutions together with the XGP will enable efficient low-cost 10 Gigabit Ethernet direct multi-port MAC to optical module interconnects with only ***PC board traces between")***.

For claim 17:

The method of claim 11, wherein the device-to-device interconnection comprises a cable (See Figure 3.10 or 4, Opto, Optical interfaces, typically connected by cable).

For claim 18:

A system comprising:

a physical layer communication device to transmit data between a transmission medium and a media independent interface (MII) at a data rate (see Figure 1, MII interfaces, XGMII); and

a communication device comprising:

a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection (see page 8, Figure 3.10 or 4); and

logic to vary the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection (Variance of data rate is a functional limitation, because no structural element of the logic was claimed in the claim, therefore reference only need to be capable varying the data rate. The reference is a product note using instruments to test 10GB Ethernet, where the instrument(s) is capable of generating % main clock rate (see 71612C technical specifications, page 7, sub clock & data Outputs, Specifications: Frequency range main clock rate), therefore, the instrument will be able to generate and capture various data rates on the XAUI interface data lines) when viewed in conjunction with the description of, "The XAUI inputs of the device under test may be driven single-ended, for example by the Agilent Technologies 71612C pattern generator *sub-rate* outputs, ...", page 10, last Para).

For claim 19:

The system of claim 18 (see supra for discussion), wherein the physical layer communication device is adapted to transmit data between the MII and a fiber optic cable (see Figure 3, 4, 5 or 6, Optical interfaces from 10 G serDes).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agilent in view of Samudrala (US 2005/0013311 Al).

Agilent teaches everything (for discussion see claim 19, supra) except for connecting the optical port to a switch fabric.

The general concept of connecting 10 GB/sec to switch fabric is well known in the art as illustrated by Samudrala et al (Fig. 5, Ingress Fabric port 7 or 8).

It would have been obvious to one skilled in the art at the time of the invention to connect optical output of Agilent to Asymmetric switch of Samudrala et al in order to have lower rate (i.e. at 1 Gb/s and 2 Gb/s rates) device interconnections as taught in Samudrala et al (Figure 5, egress ports of 0-3 (1 Gb/s port) and port 4-5 (2 Gb/s), and Port 6-7 (10 Gb/S).

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agilent publication (Agilent Technologies product note) in view January 1997 National Semiconductor publication (pages 1-14, Jan 1997).

Agilent teaches everything (for discussion see claim 19 supra) except for adapting physical communication device to transmit data between the MII and a twisted wire pair cable.

The general concept of adapting physical communication device to transmit data between the MII

and a twisted wire pair cable is well known in the art as illustrated by National semiconductor publication as shown in page 12, with RJ45 Jack connection (are always connected by pair of wires)).

It would have been obvious to one skilled in the art at the time of invention to modify Agilent application note to adapt physical communication device to transmit data between the MII and a twisted wire pair cable in order to be back word compatible with 10/100 Mb/S PHY devices as taught in National semiconductor publication. (Page 9, second square bullet point).

5. Claim 21-29 and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agilent publication in view of Actel Application Notes (a copy provided):

For Claims 21 and 30:

Agilent publication teaches:

a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection (page 8, Figure 4, Plurality of

data lines two differential transmitting and two differential receiving); and

logic to vary the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection (Variance of data rate is a functional limitation, because no structural element of the logic was claimed in the claim, therefore reference only need to be capable varying the data rate. The reference is a product note using instruments to test 10GB Ethernet, where the instrument(s) is capable of generating 1/4 main clock rate (see 71612C technical specifications, page 7, sub clock & data Outputs, Specifications: Frequency range **1/4** main clock rate), therefore, the instrument will be able to generate and capture various data rates on the XAUI interface data lines) when viewed in conjunction with the description of, "The XAUI inputs of the

device under test may be driven single-ended, for example by the Agilent Technologies 71612C pattern generator *sub-rate* outputs, ...", page 10, last Para).

Therefore, Agilent publication teaches every thing except for using state machine at least one of transmit and receive data at a data rate.

The general concept of using sate machine to transmit and receive data is well known as illustrated by Actel publication (see block diagram on page 2, Figure 1 and 2, Reset Sync and with block diagrams is a state machine, also see Figure 3, transmitter block diagram and Figure 5, receiver Block diagram along with Figure 6, SYNC_FSM state Diagram).

It would have obvious to one in skilled in art at the time of invention to modify Agilent publication to use the state machine to transmit and receive data in order to implement the device in the programmable logic design as taught in Actel publication (page 1, column 2, second Para, lines 1-2, "There are several challenges in implementing an 8B/10bB encoder/decoder (ENDEC) in a programmable logic device.").

For Claims 22 and 31:

The device of claim 21 (see supra for discussion), wherein each data lane interface is

associated with a first differential pair to transmit a serial data signal and a second differential pair to receive a serial data signal (See Agilent publication, Figure 4, 2 (Differential) X 2 (Tx & Rx)).

For claims 23 and 32:

The device of claim 22 (see claim 22 supra) wherein the plurality of data lane interface are capable of transmitting data to and receiving data from a 10 gigabit attachment unit interface (See Figure 7, XAUI interface).

For claims 24 and 33:

The device of claim 21 (see supra for discussion), wherein the data rate is controlled by a frequency of a first clock signal, and wherein the device further comprises:

a plurality of 8B '10B decoders; each 8B 10B decoder being associated with one of the data lane interfaces, each 8B 10B decoder being capable of decoding one eight bit byte from a differential pair at a rate controlled by a frequency of a second

clock signal (Figure 5 or 6, showing of 8B/10 encoder/decoder serdes for each data lanes); and

logic to vary the frequency of the first clock signal based, at least in part, upon a number of the data lane interfaces actively receiving serial data from the device-to-device interconnection (to strobe the received data into a register, the clock frequency has to be changed).

For claims 25 and 34: The device of claim 21, wherein the data rate is controlled by a frequency of a first clock signal, and wherein the device further comprises:

a plurality of 8B 10B encoders, each 8B 10B encoder being associated with one of the data lane interfaces, each 8B 10B encoder being capable of encoding one eight bit byte of the fixed length data signal for transmission to a differential pair at a rate controlled by a second clock signal (Figure 5 or 6, showing of 8B/10B encoder/decoder serdes for each of data lanes); and

logic to vary the frequency of the first clock signal based, at least in part, upon a number of the data lane interfaces actively transmitting serial data from to the device to device interconnection (to strobe data to be transmitted, the strobe clock frequency has to be changed).

For claim 26:

The device of claim 21 (see supra for discussion), wherein the device further comprises a MAC to at least one of transmit data to and receive data from the state machine at the data rate (Agilent publication, see figure 4, MAC with RCS).

For claim 27:

The device of claim 21 (see supra for discussion), wherein the device further comprises a physical layer communication device to at least one of transmit data to and receive data from the state machine at the data rate (See Agilent publication, page 8, Figure 4, Optical SCD connector technology).

For claim 28:

The device of claim 21, wherein the device-to-device interconnection comprises printed circuit board traces (see page 8, Figure 4, "Robust CML differential, un-clocked interface allows trace lengths of 18" on FR4", which are PCB copper traces).

For claim 29:

The method of claim 21 (see supra for discussion); wherein the device-to-device interconnection comprises a cable (Figure 5 or 6, Optical connector is a cable).

Conclusion

6. **ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will

expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yasin Barqadle whose telephone number is 571-272-3947. The examiner can normally be reached on 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenn Burgess can be reached on 571-272-3949. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Information regarding the status of an application may be obtained form the Patent Application Information Retrieval

(PAIR) system. Status information for published applications may be obtained from either private PAIR or public PAIR system. Status information for unpublished applications is available through private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YB

Art Unit 2153

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